An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration

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Abstract This paper analyzes a pseudo-differential dynamic comparator with a dynamic pre-amplifier as shown in figure 1. The transient gain of a dynamic pre-amplifier is derived and well matched with the simulation results. Based on the calculated gain, a load capacitance calibration method is analyzed. This analysis well estimates input-referred compensated voltage of each digital calibration code. The influence of PVT variation is also figured out. This analysis shows a dynamic comparator is sensitive to input common-mode voltage variation as shown in figure 2. The analyzed comparator uses 90-nm CMOS technology as an example.

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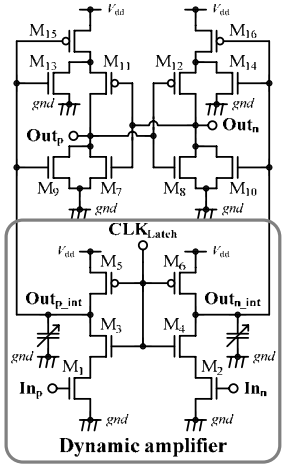

Fig. 1 A schematic of a comparator.

$$\mathrm{SNDR}_{\mathrm{decrease}} = -10\log\left(1+\frac{12}{V_{\mathrm{q}}^2}\sigma_{\mathrm{V}}^2\right)$$

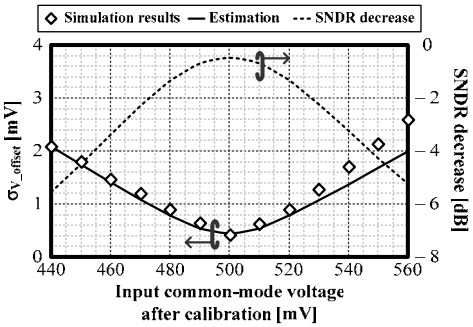

Fig. 2 The influence of input common-mode voltage variation on the capacitance calibration (1 LSB = V_{q} = 4.5 mV).